A1 cont'd.

34b, 34c, and 34d. Liner segment 34a is joined to originating segment 31 by a first turn 33a and is joined to linear segment 34b by a second turn 33b. Linear segment 34b is joined to linear segment 34c by a third turn 33c, and linear segment 34c is joined to linear segment 34d by a fourth turn 33d. The serpentine conductor is terminated, at terminating segment 32, in the substantially rectangular, conductor 40 formed as a planar pad.

Please replace the paragraph beginning on Page 9, line 5 with the following amended paragraph:

A2

In an exemplary embodiment, tuning capacitance conductor 40 may be configured in rectangular form, as depicted in Figure 2. However, those skilled in the art will recognize that tuning capacitance conductor 40 may assume other geometries, including square, circular, triangular, etc. and may adopt an irregular shape. However, in order for conductor 40 to instantiate a capacitance at F_o, conductor 40 must subtend an appropriate area on the PCB and must be positioned in some proximity to a second conductor. In the arrangement of Figure 2, conductor 40 as positioned to be proximate a ground plane 60. In one embodiment (Figure 2A), conductor 40 may be deposited on the top surface of the PCB, diametrically opposed a ground plane that is deposited on the bottom surface. In this configuration, the tuning capacitance is formed by conductor 40, ground plane 60, and intervening (between conductor 40 and ground plane 60) thickness of the dielectric PCB 100. In an alternative, but perhaps less effective embodiment (Figure 2B), ground plane 60 may envelop portions of conductor 40 on the top surface of PCB 100. The essence is that conductor 40 is to form one "plate" of a capacitor, and the ground plane on system board forms the second "plate." In this manner, serpentine conductor 30 and conductor 40 effectively form a series LC network, at F_0, between pad 20 and GND. Note, however, that there exists no electrical continuity by virtue of LC network between pad 20 and GND.

Please replace the paragraph beginning on Page 10, line 1 with the following amended paragraph:

A3

For example, in a situation in which 400 MHz noise must be prevented or blocked from appearing at the B^+ pin of an ASIC on the system board, where, for example, a discrete 0.01 uf bypass capacitor as deployed, a simulation effort was conducted to determine the corresponding